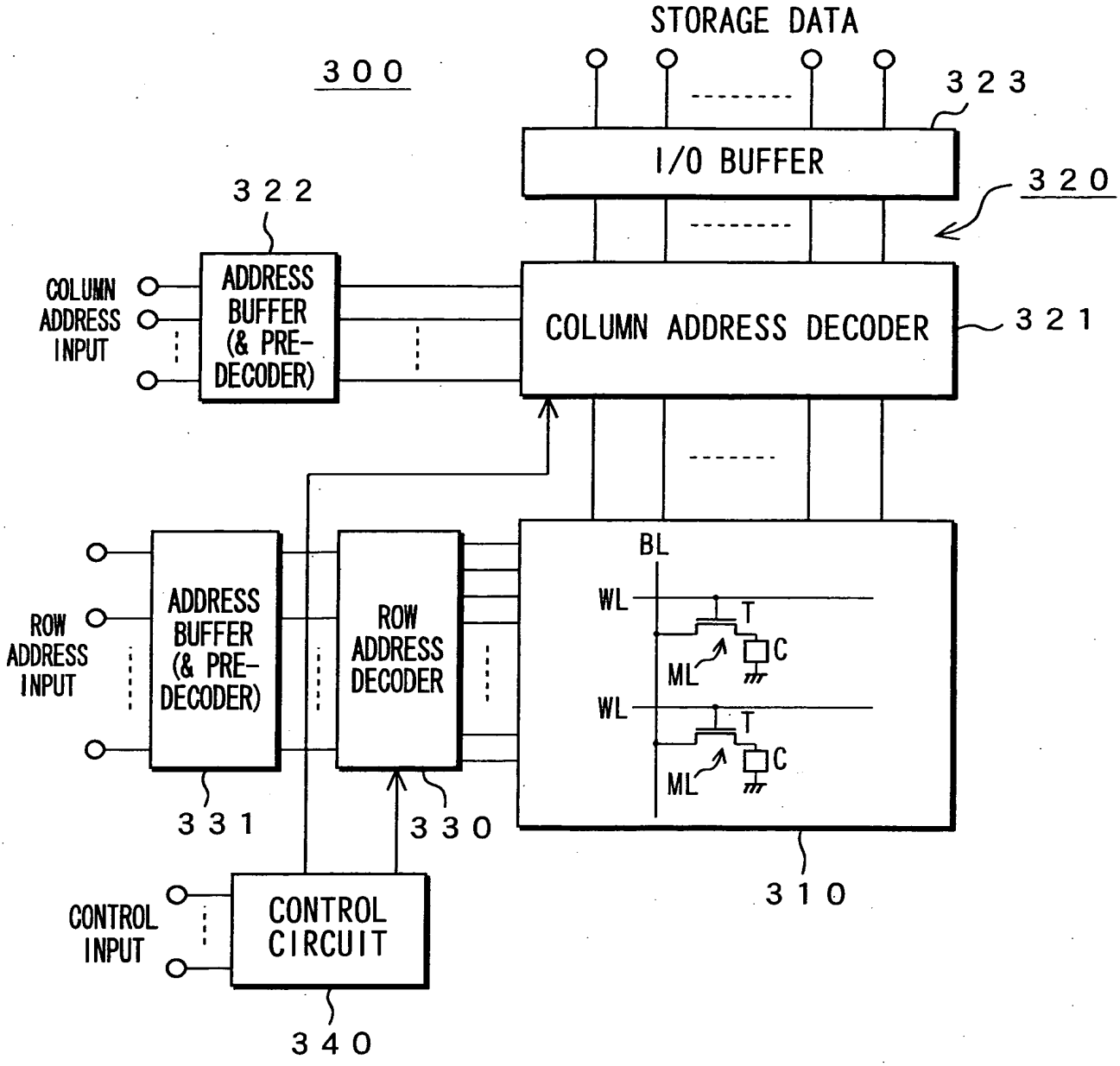
10/531005

FIG. 1



F I G. 2

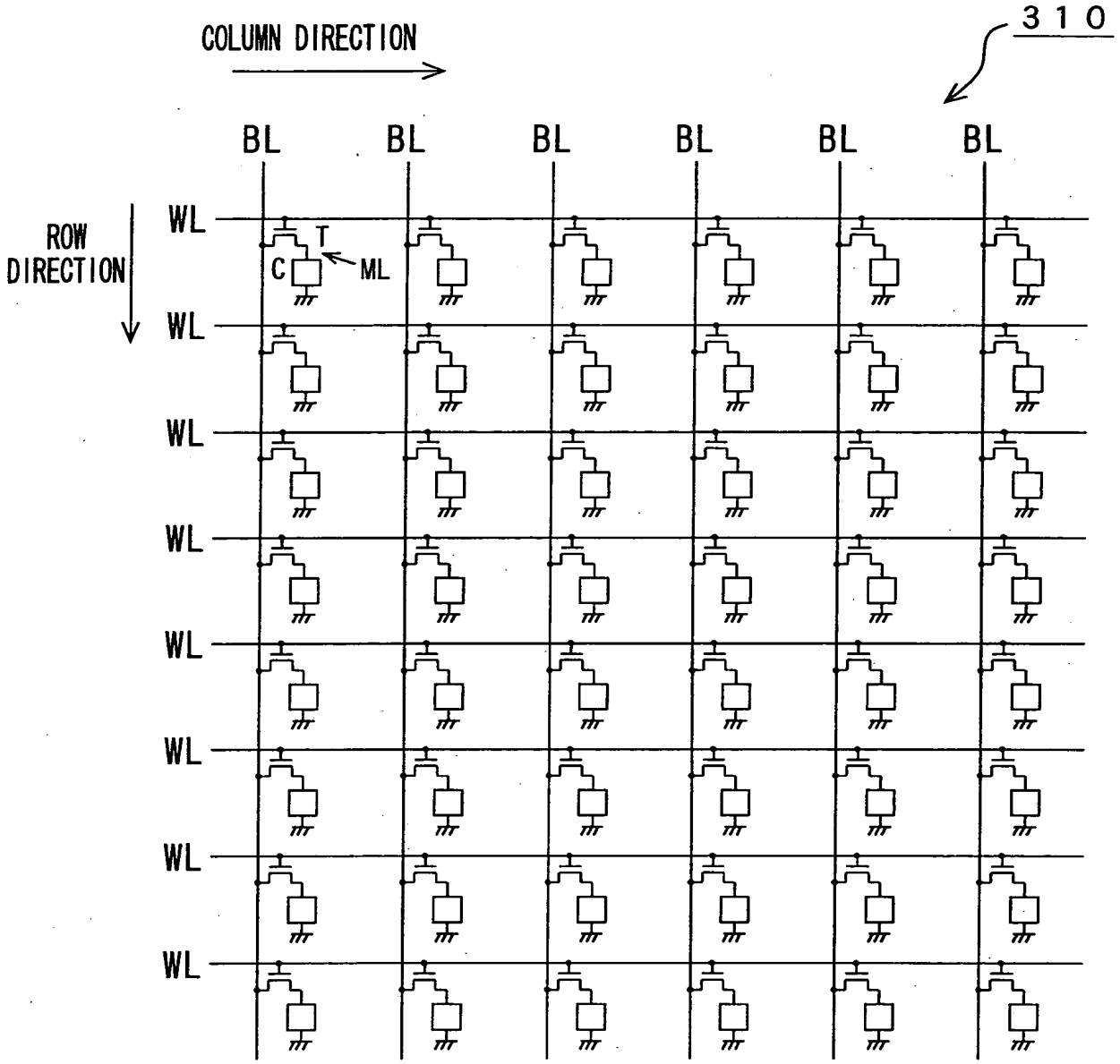

COLUMN DIRECTION
310
BL
BL
BL
BL
BL
BL
ROW DIRECTION
WL
WL
WL
WL
WL
WL
WL
WL
T
C
ML

FIG. 3

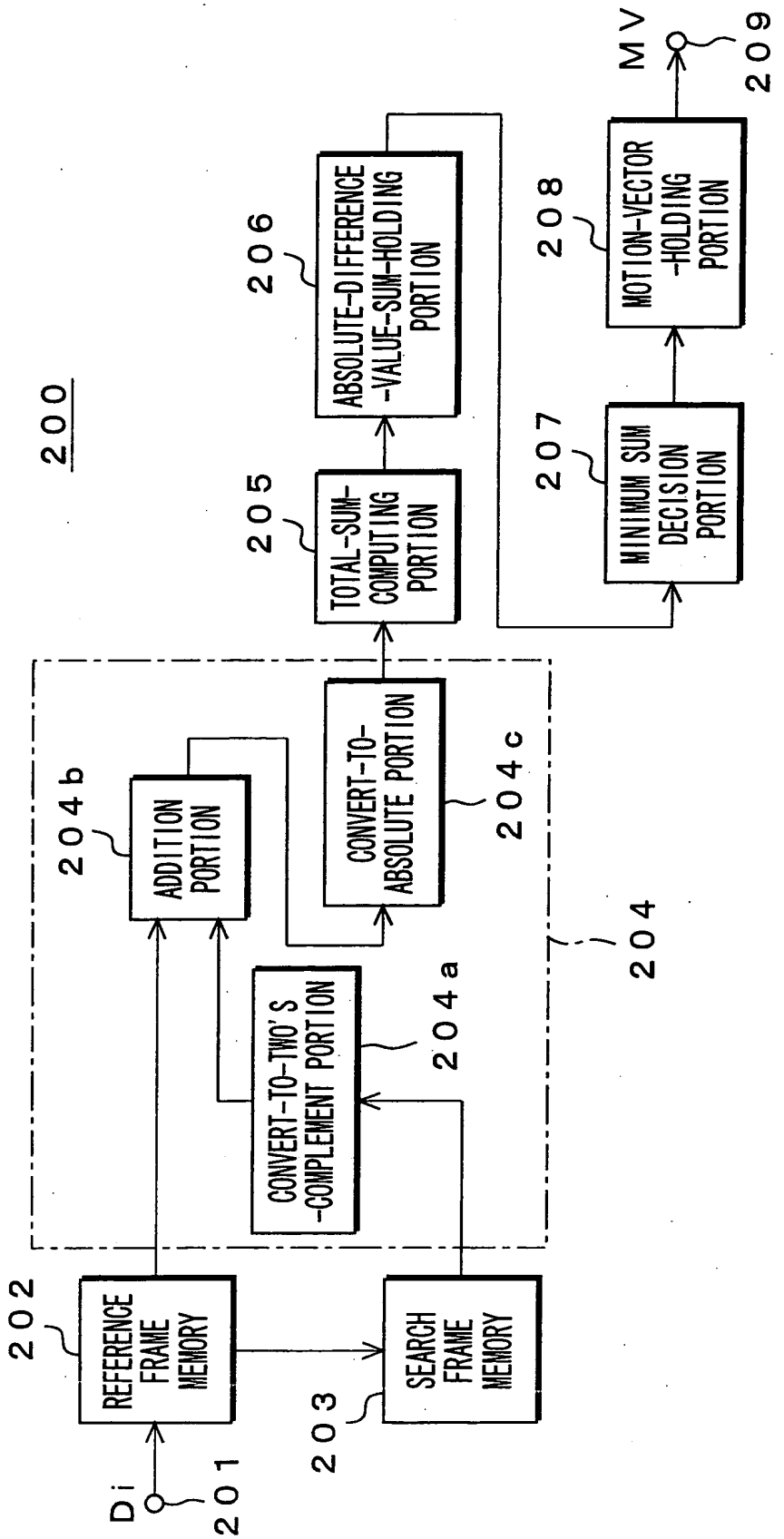

200
Di
201
202
REFERENCE FRAME MEMORY
203
SEARCH FRAME MEMORY
204
204a
CONVERT-TO-TWO'S -COMPLEMENT PORTION
204b
ADDITION PORTION
204c
CONVERT-TO-ABSOLUTE PORTION
205
TOTAL-SUM-COMPUTING PORTION
206
ABSOLUTE-DIFFERENCE-VALUE-SUM-HOLDING PORTION
207
MINIMUM SUM DECISION PORTION
208
MOTION-VECTOR-HOLDING PORTION
MV
209

FIG. 4

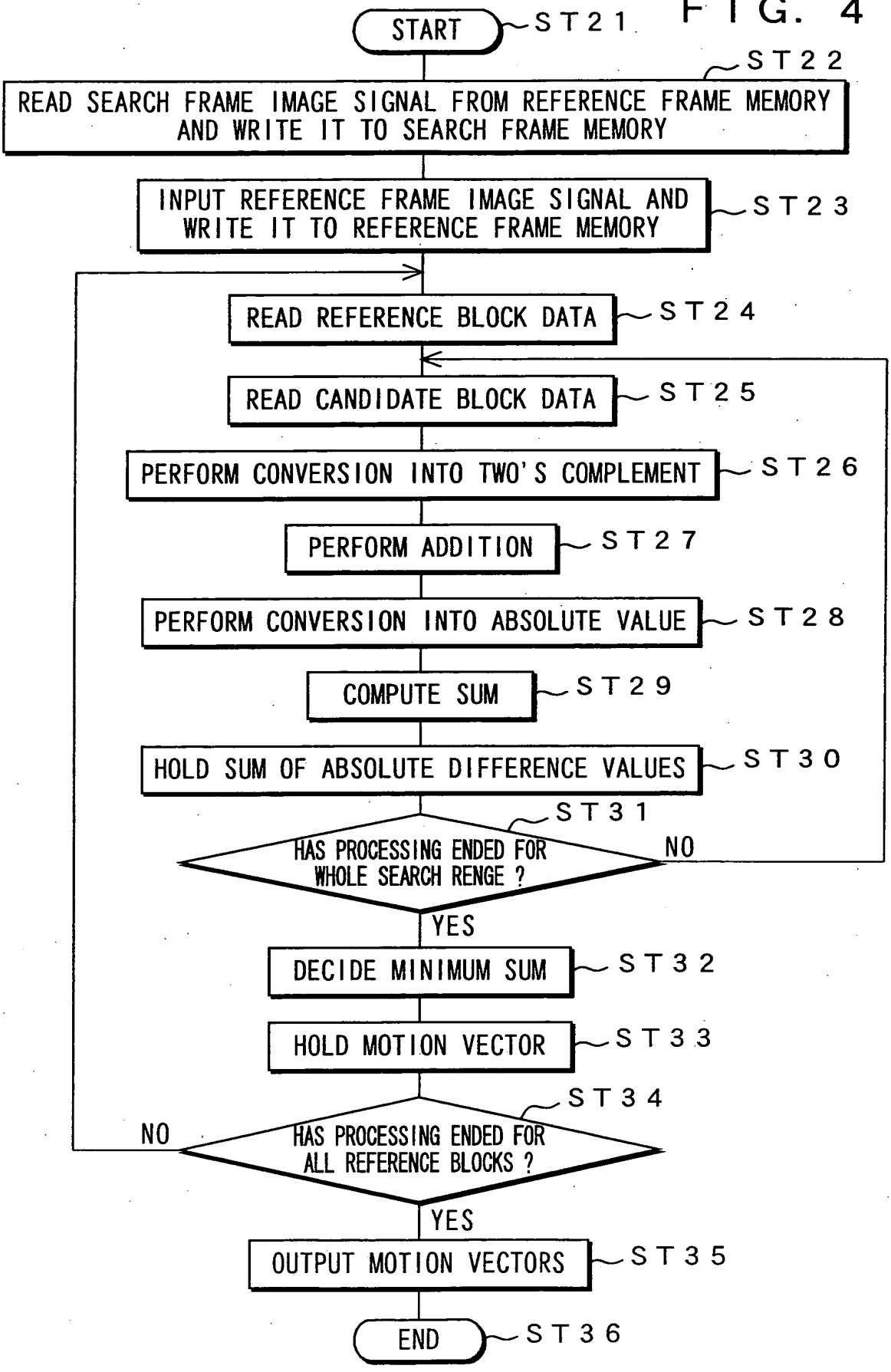

START
ST21
READ SEARCH FRAME IMAGE SIGNAL FROM REFERENCE FRAME MEMORY AND WRITE IT TO SEARCH FRAME MEMORY
ST22
INPUT REFERENCE FRAME IMAGE SIGNAL AND WRITE IT TO REFERENCE FRAME MEMORY
ST23
READ REFERENCE BLOCK DATA
ST24
READ CANDIDATE BLOCK DATA
ST25
PERFORM CONVERSION INTO TWO'S COMPLEMENT
ST26
PERFORM ADDITION
ST27
PERFORM CONVERSION INTO ABSOLUTE VALUE
ST28
COMPUTE SUM
ST29
HOLD SUM OF ABSOLUTE DIFFERENCE VALUES
ST30
HAS PROCESSING ENDED FOR WHOLE SEARCH RENGE ?
ST31
NO
YES
DECIDE MINIMUM SUM
ST32
HOLD MOTION VECTOR
ST33
HAS PROCESSING ENDED FOR ALL REFERENCE BLOCKS ?
ST34
NO
YES
OUTPUT MOTION VECTORS
ST35
END
ST36

FIG. 5

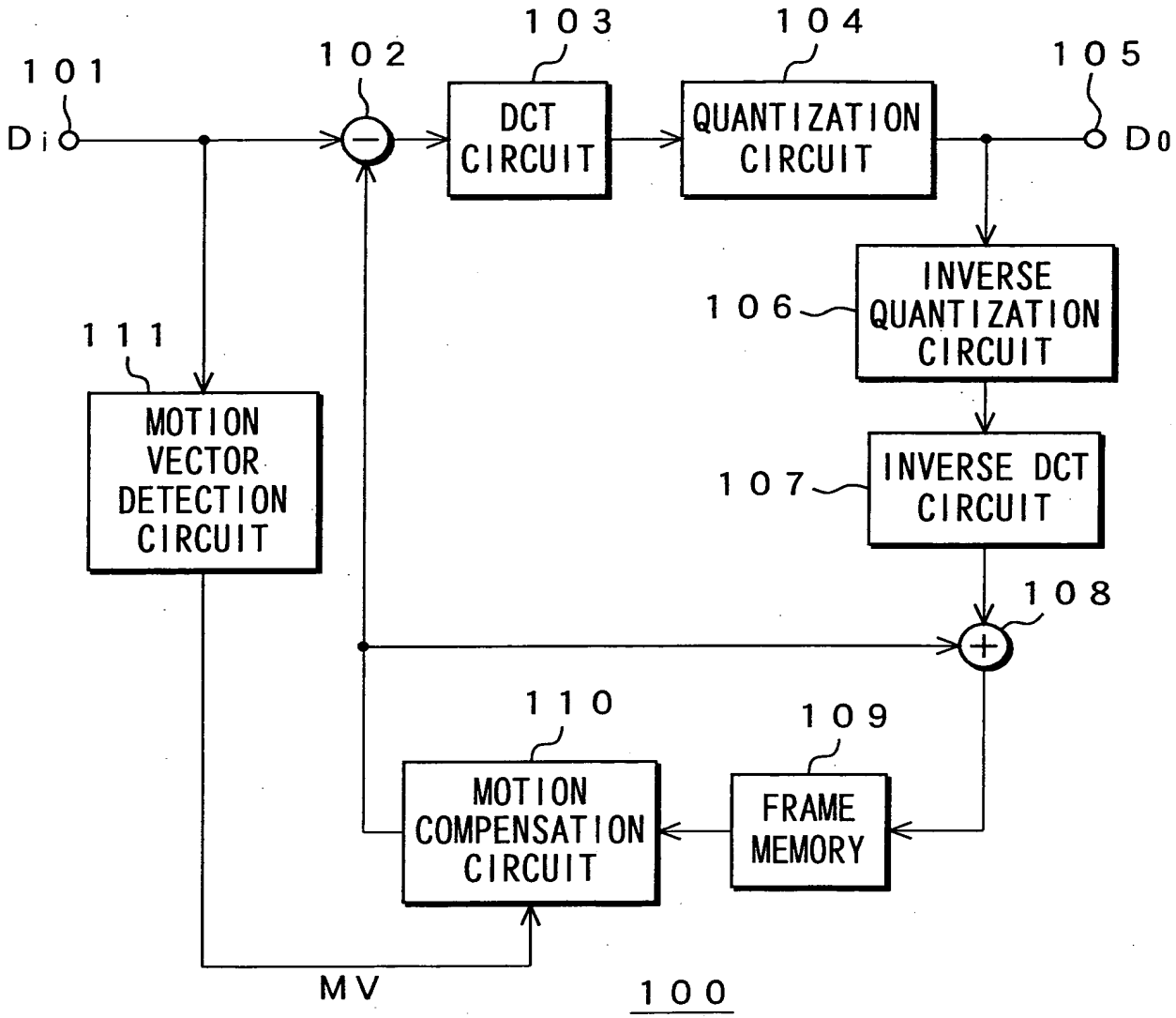

101
Di
102
103
DCT CIRCUIT
104
QUANTIZATION CIRCUIT
105
Do
106
INVERSE QUANTIZATION CIRCUIT
107
INVERSE DCT CIRCUIT
108
111
MOTION VECTOR DETECTION CIRCUIT
110
MOTION COMPENSATION CIRCUIT
109
FRAME MEMORY
MV
100

FIG. 6

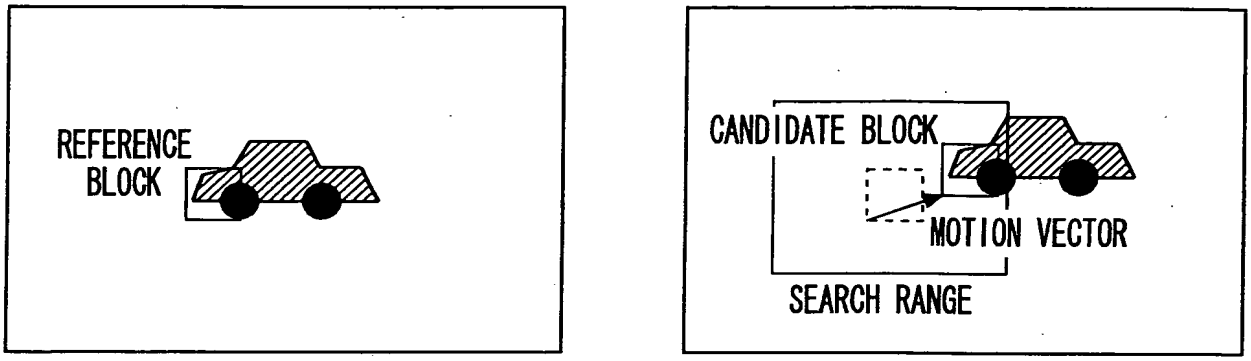


FIG. 7A

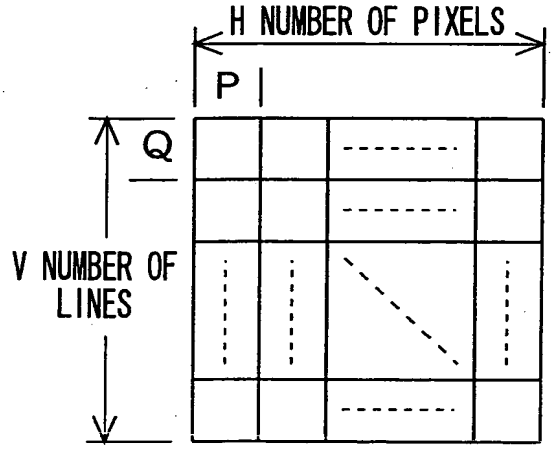


FIG. 7B

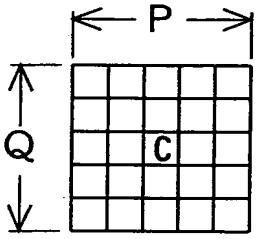


FIG. 8A

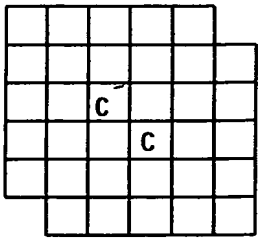


FIG. 8B

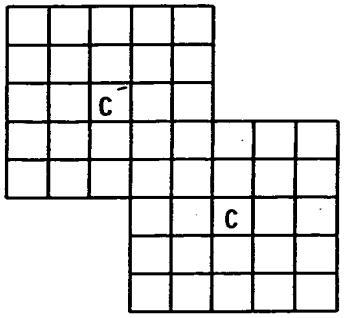


FIG. 8C

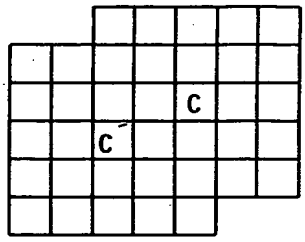


FIG. 9

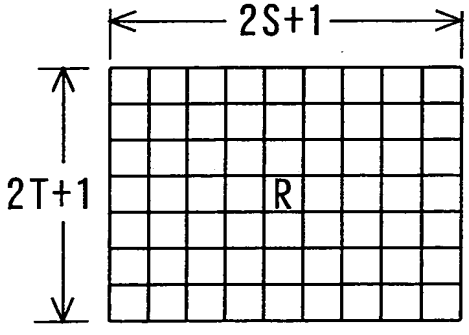


FIG. 10

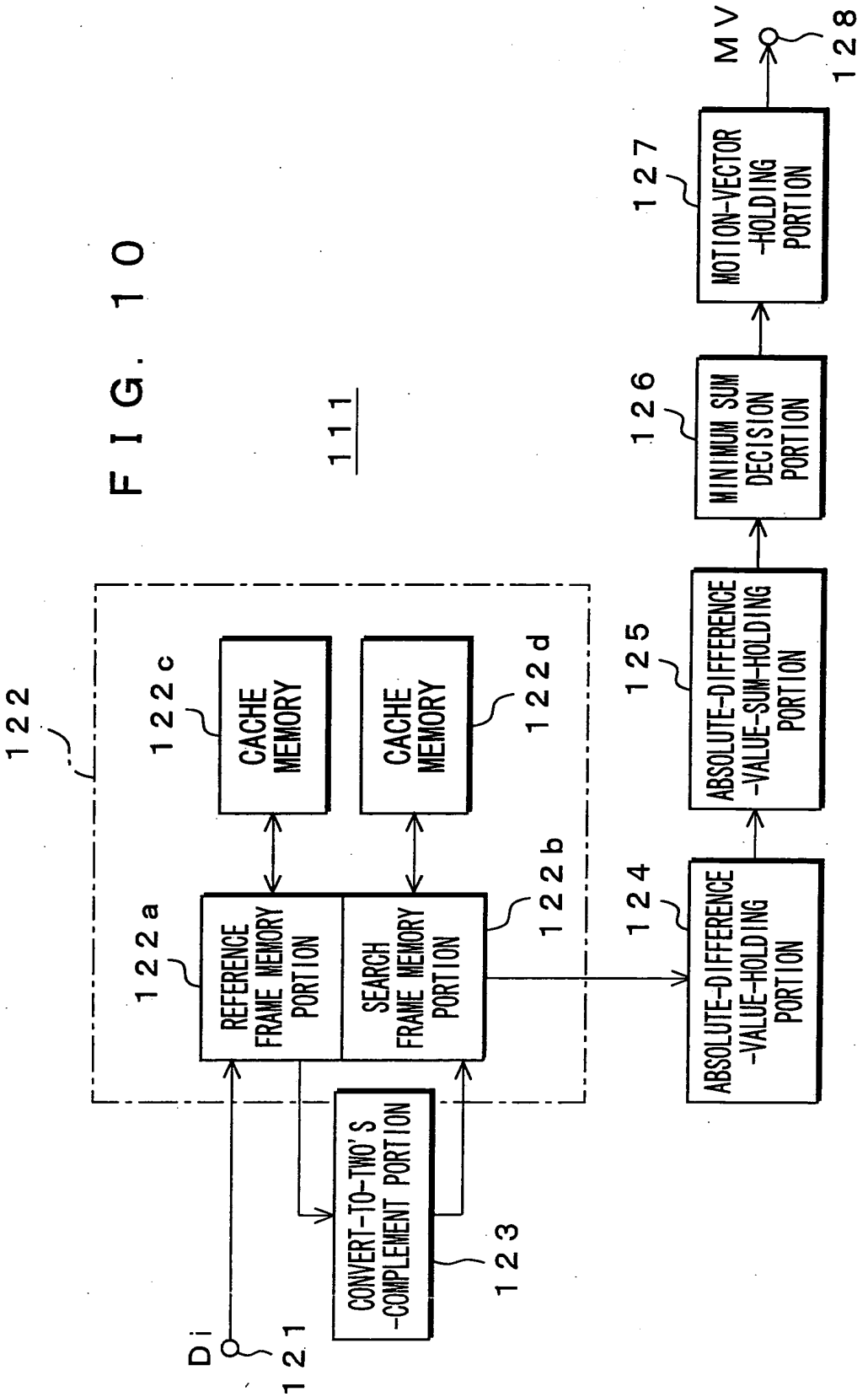

111
122
122a
REFERENCE FRAME MEMORY PORTION
SEARCH FRAME MEMORY PORTION
122b
122c
CACHE MEMORY
122d
CACHE MEMORY
123
CONVERT-TO-TWO'S -COMPLEMENT PORTION
121
Di
124
ABSOLUTE-DIFFERENCE -VALUE-HOLDING PORTION
125
ABSOLUTE-DIFFERENCE -VALUE-SUM-HOLDING PORTION
126
MINIMUM SUM DECISION PORTION
127
MOTION-VECTOR -HOLDING PORTION
MV
128

FIG. 11

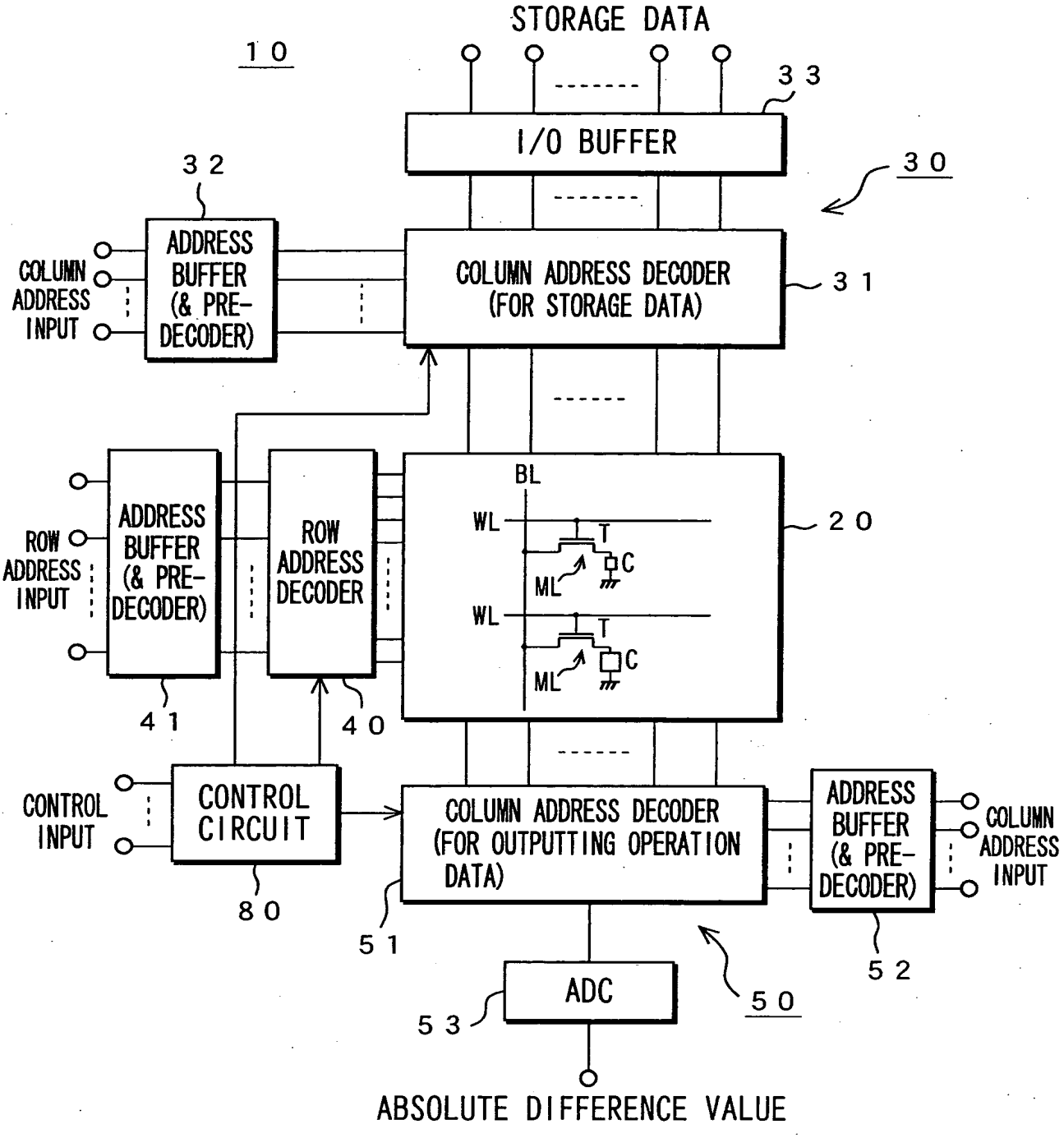

STORAGE DATA
10
33
I/O BUFFER
30
32
ADDRESS BUFFER (& PRE-DECODER)
COLUMN ADDRESS INPUT
COLUMN ADDRESS DECODER (FOR STORAGE DATA)
31
BL
WL
T
C
ML
20
ROW ADDRESS INPUT
ADDRESS BUFFER (& PRE-DECODER)
ROW ADDRESS DECODER
41
40
CONTROL INPUT
CONTROL CIRCUIT
80
COLUMN ADDRESS DECODER (FOR OUTPUTTING OPERATION DATA)
51
ADDRESS BUFFER (& PRE-DECODER)
COLUMN ADDRESS INPUT
52
ADC
53
50
ABSOLUTE DIFFERENCE VALUE

FIG. 12

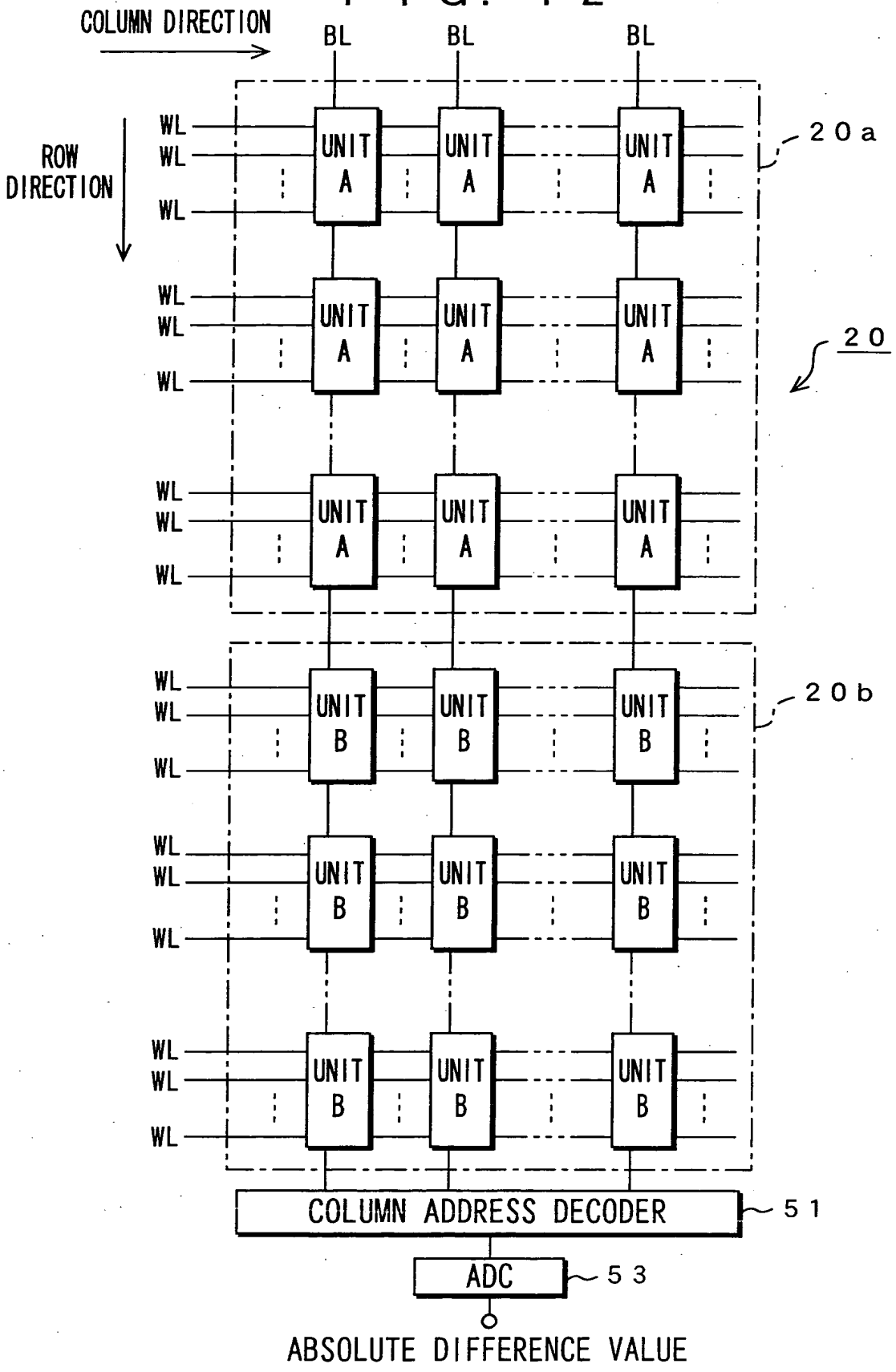

COLUMN DIRECTION
ROW DIRECTION
BL
BL
BL
WL
UNIT A
20a
20
UNIT B
20b
COLUMN ADDRESS DECODER
51
ADC
53
ABSOLUTE DIFFERENCE VALUE

FIG. 13A

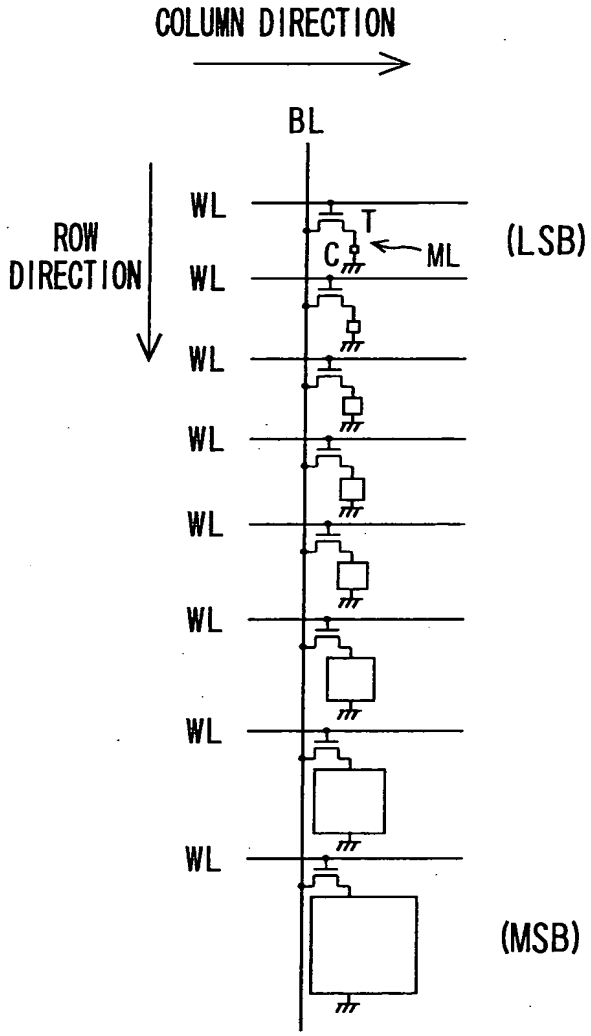


FIG. 13B

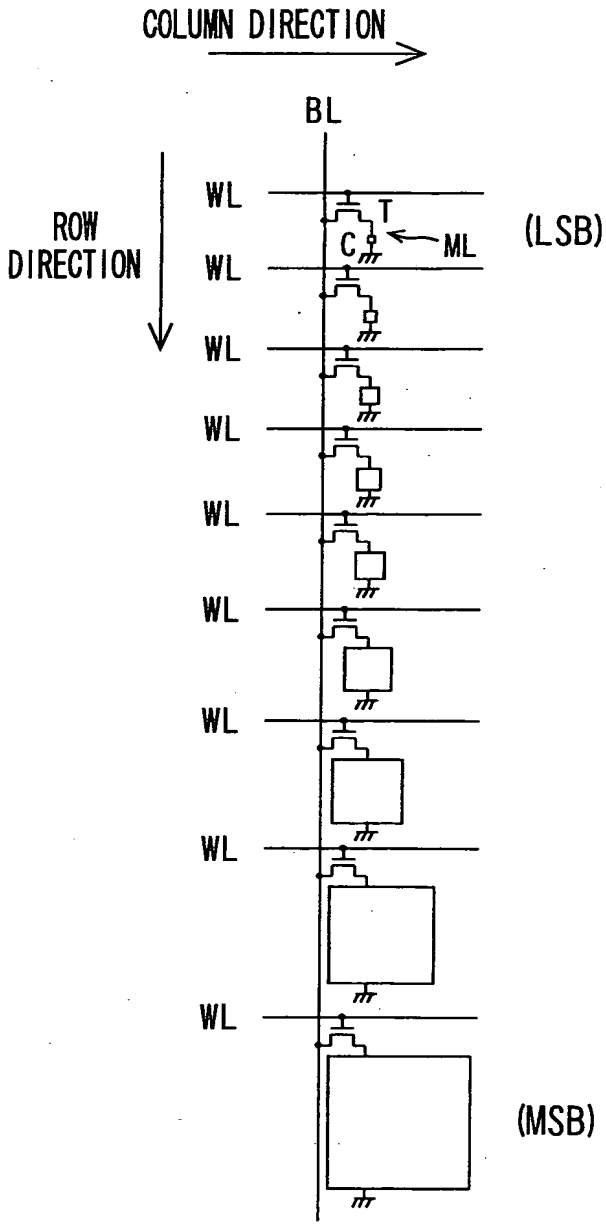


FIG. 14

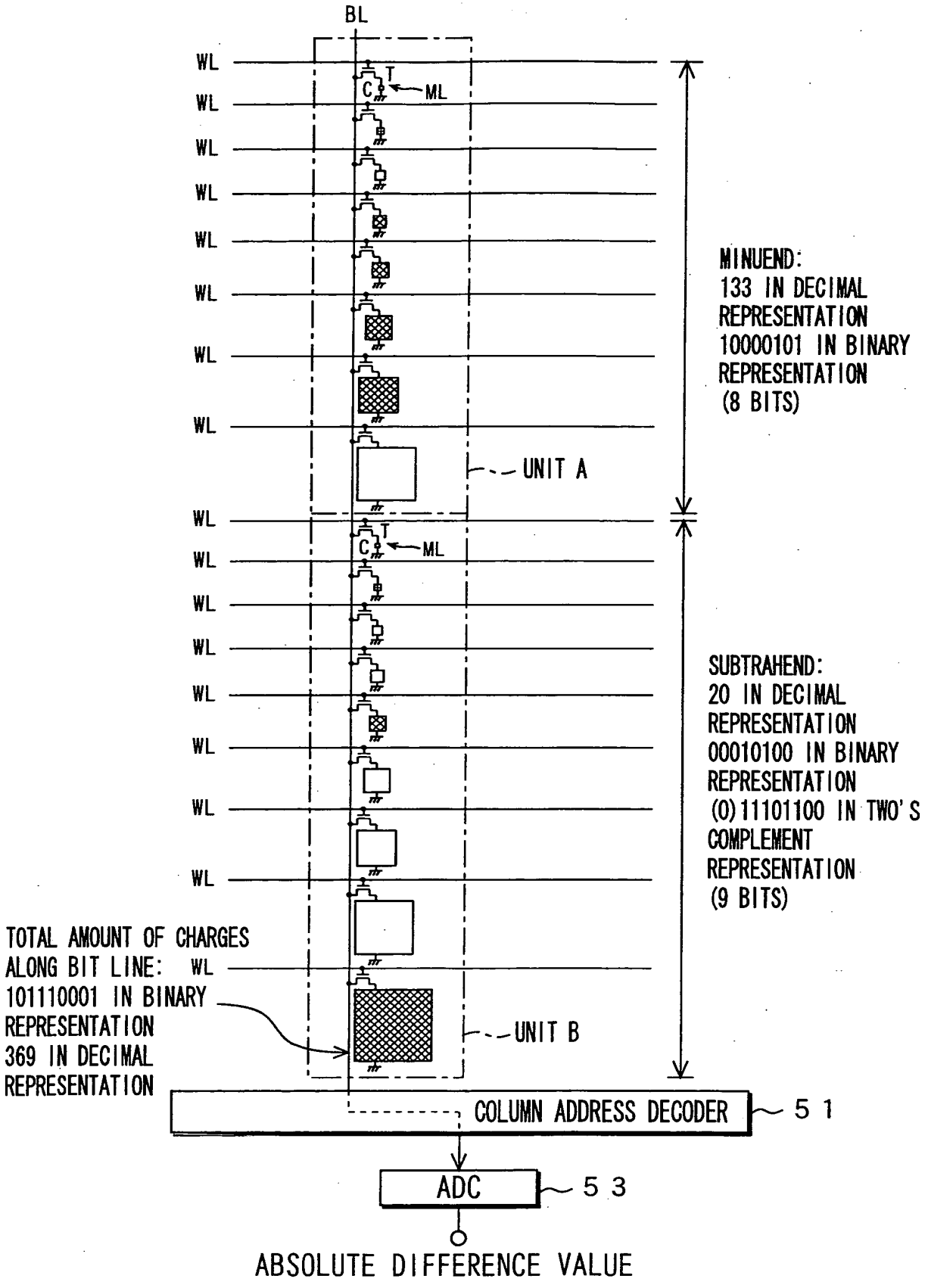

BL
WL
T
C
ML
UNIT A
UNIT B
MINUEND:
133 IN DECIMAL REPRESENTATION
10000101 IN BINARY REPRESENTATION
(8 BITS)
SUBTRAHEND:
20 IN DECIMAL REPRESENTATION
00010100 IN BINARY REPRESENTATION
(0)11101100 IN TWO'S COMPLEMENT REPRESENTATION
(9 BITS)
TOTAL AMOUNT OF CHARGES ALONG BIT LINE:
101110001 IN BINARY REPRESENTATION
369 IN DECIMAL REPRESENTATION
COLUMN ADDRESS DECODER
51
ADC
53
ABSOLUTE DIFFERENCE VALUE

FIG. 15

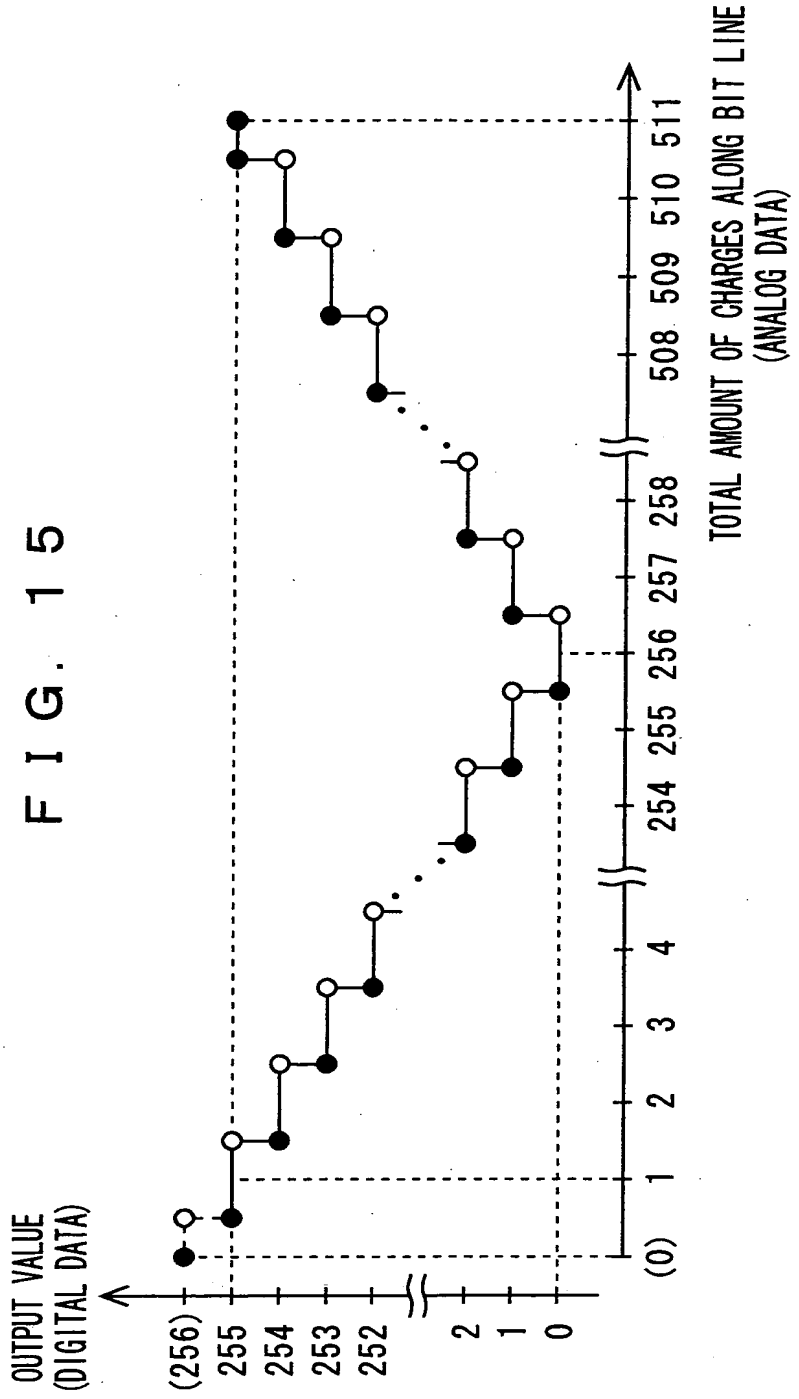

OUTPUT VALUE
(DIGITAL DATA)
(256)
255
254
253
252
2
1
0
(0) 1 2 3 4 254 255 256 257 258 508 509 510 511
TOTAL AMOUNT OF CHARGES ALONG BIT LINE
(ANALOG DATA)

FIG. 16

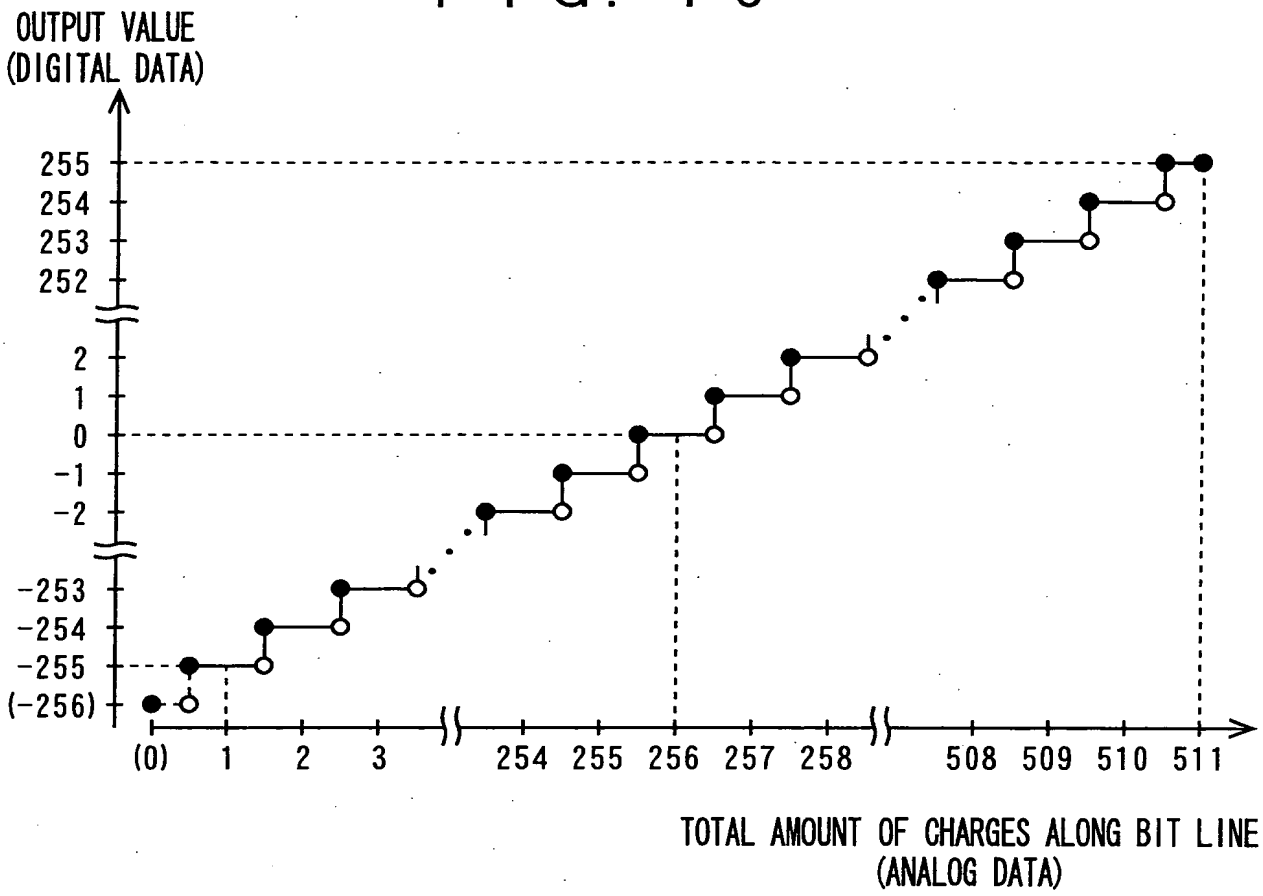

OUTPUT VALUE
(DIGITAL DATA)
255
254
253
252
2
1
0
-1
-2
-253
-254
-255
(-256)
(0)
1
2
3
254
255
256
257
258
508
509
510
511
TOTAL AMOUNT OF CHARGES ALONG BIT LINE
(ANALOG DATA)

FIG. 17

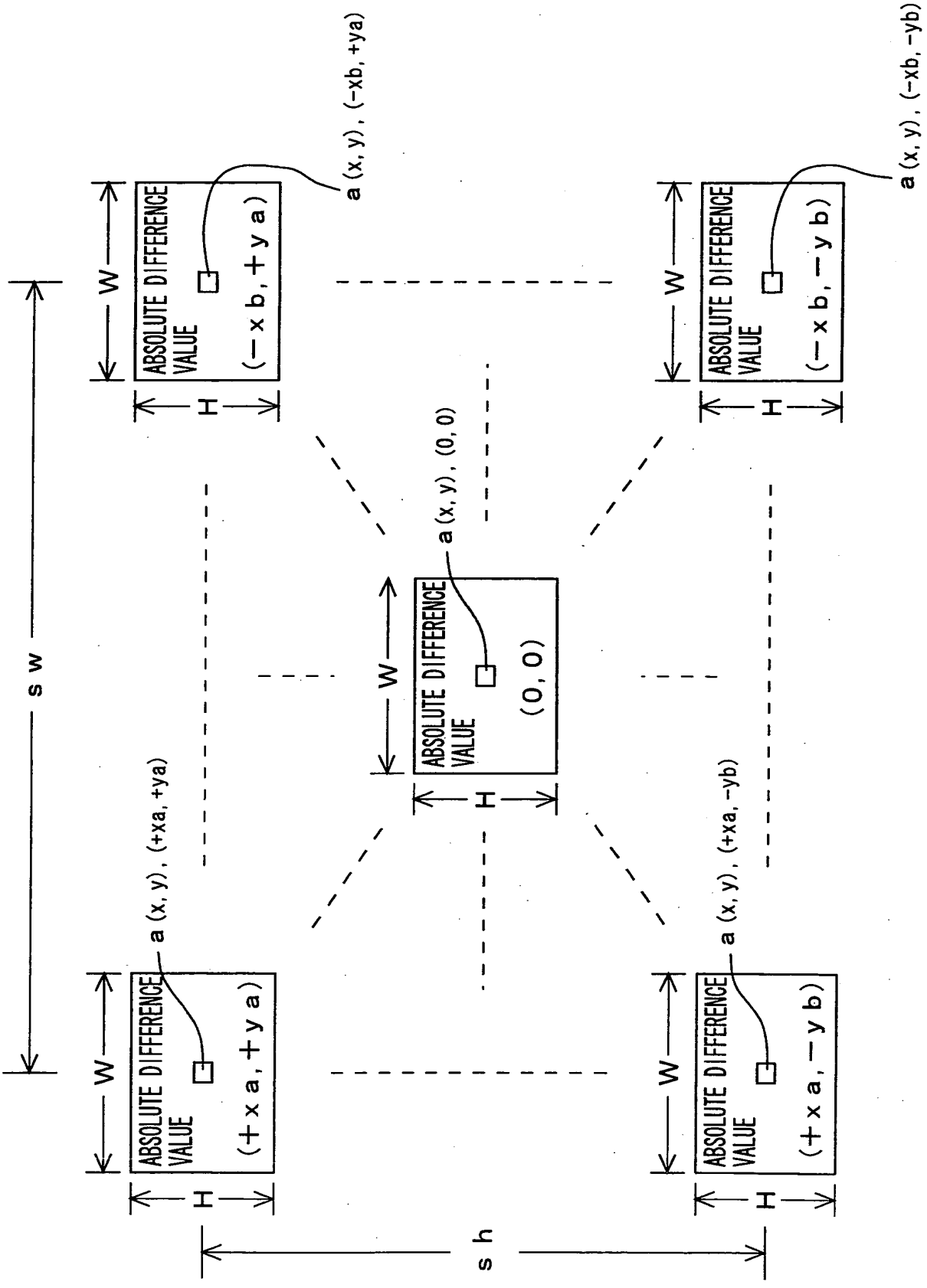

a (x, y), (−xb, +ya)
ABSOLUTE DIFFERENCE VALUE
(−x b, +y a)
a (x, y), (−xb, −yb)
ABSOLUTE DIFFERENCE VALUE
(−x b, −y b)
a (x, y), (0, 0)
ABSOLUTE DIFFERENCE VALUE
(0, 0)
a (x, y), (+xa, +ya)
ABSOLUTE DIFFERENCE VALUE
(+x a, +y a)
a (x, y), (+xa, −yb)
ABSOLUTE DIFFERENCE VALUE
(+x a, −y b)
W
H
sw
sh

FIG. 18

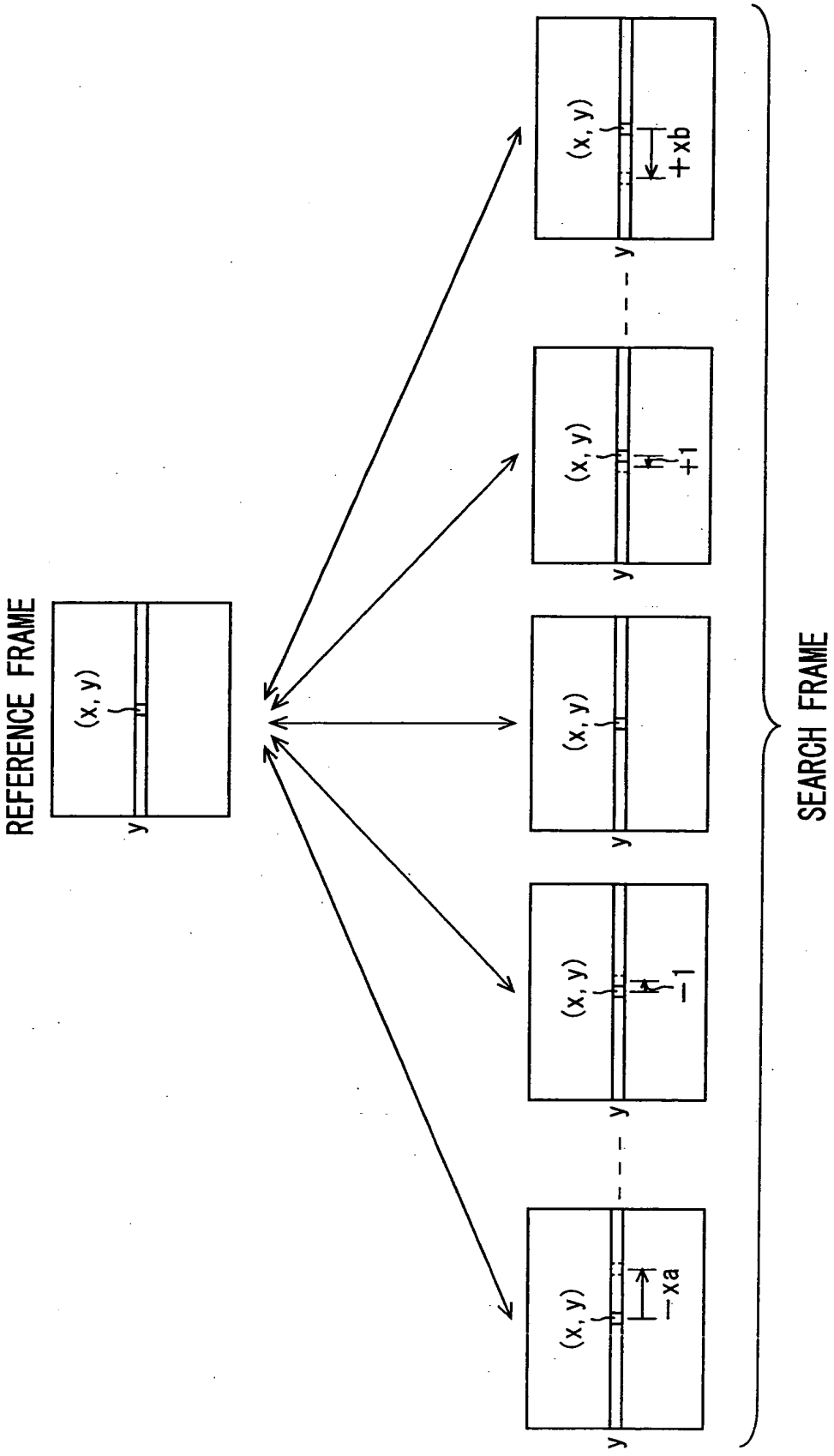


FIG. 19

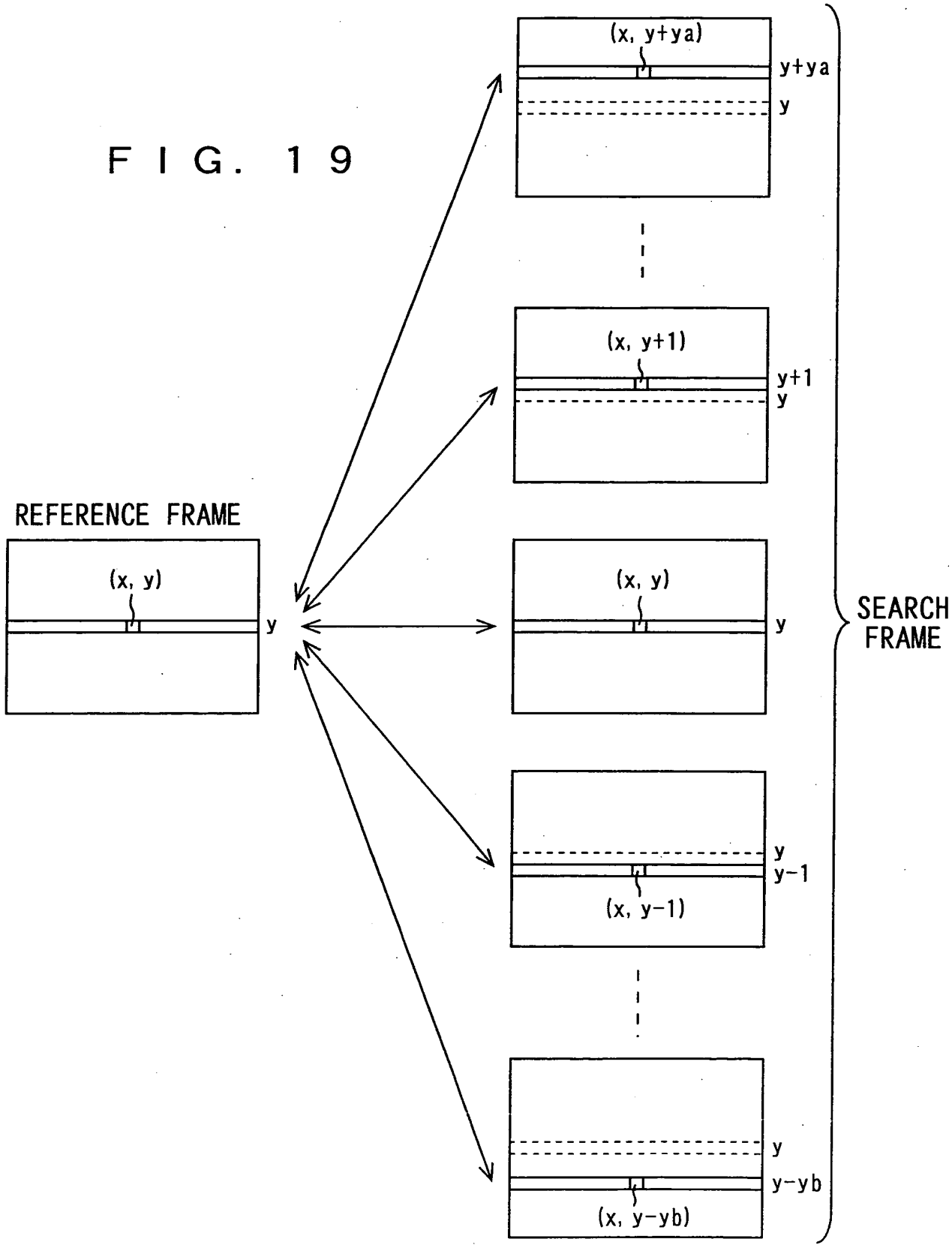

(x, y+ya)
y+ya
y
(x, y+1)
y+1
y
REFERENCE FRAME
(x, y)
y
(x, y)
y
SEARCH FRAME
y
y-1
(x, y-1)
y
y-yb
(x, y-yb)

FIG. 20

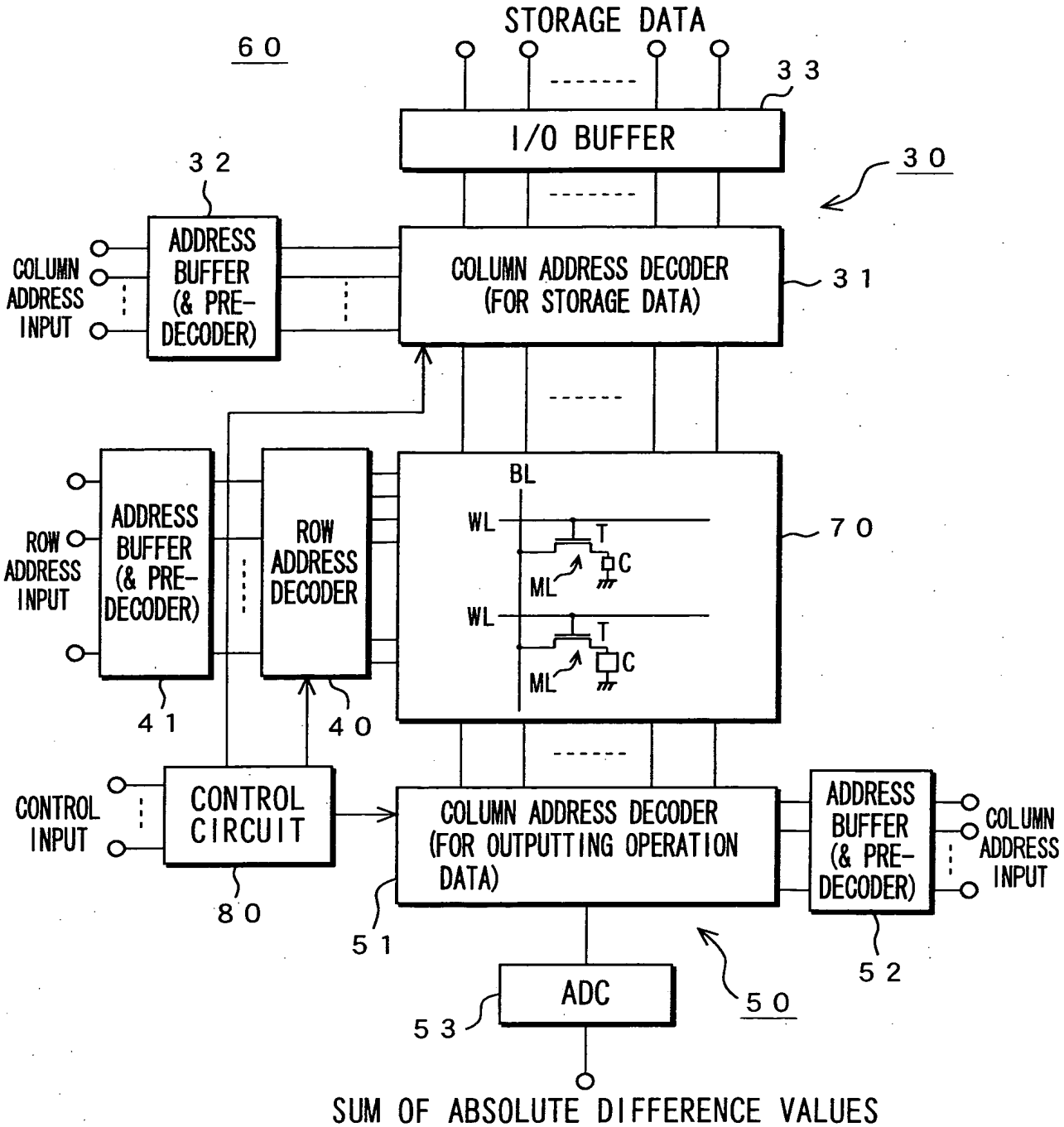

STORAGE DATA
60
33
I/O BUFFER
32
30
ADDRESS BUFFER (& PRE-DECODER)
COLUMN ADDRESS INPUT
COLUMN ADDRESS DECODER (FOR STORAGE DATA)
31
BL
WL
T
C
ML
70
ADDRESS BUFFER (& PRE-DECODER)
ROW ADDRESS INPUT
ROW ADDRESS DECODER
41
40
CONTROL INPUT
CONTROL CIRCUIT
80
COLUMN ADDRESS DECODER (FOR OUTPUTTING OPERATION DATA)
51
ADDRESS BUFFER (& PRE-DECODER)
COLUMN ADDRESS INPUT
52
ADC
53
50
SUM OF ABSOLUTE DIFFERENCE VALUES

FIG. 21

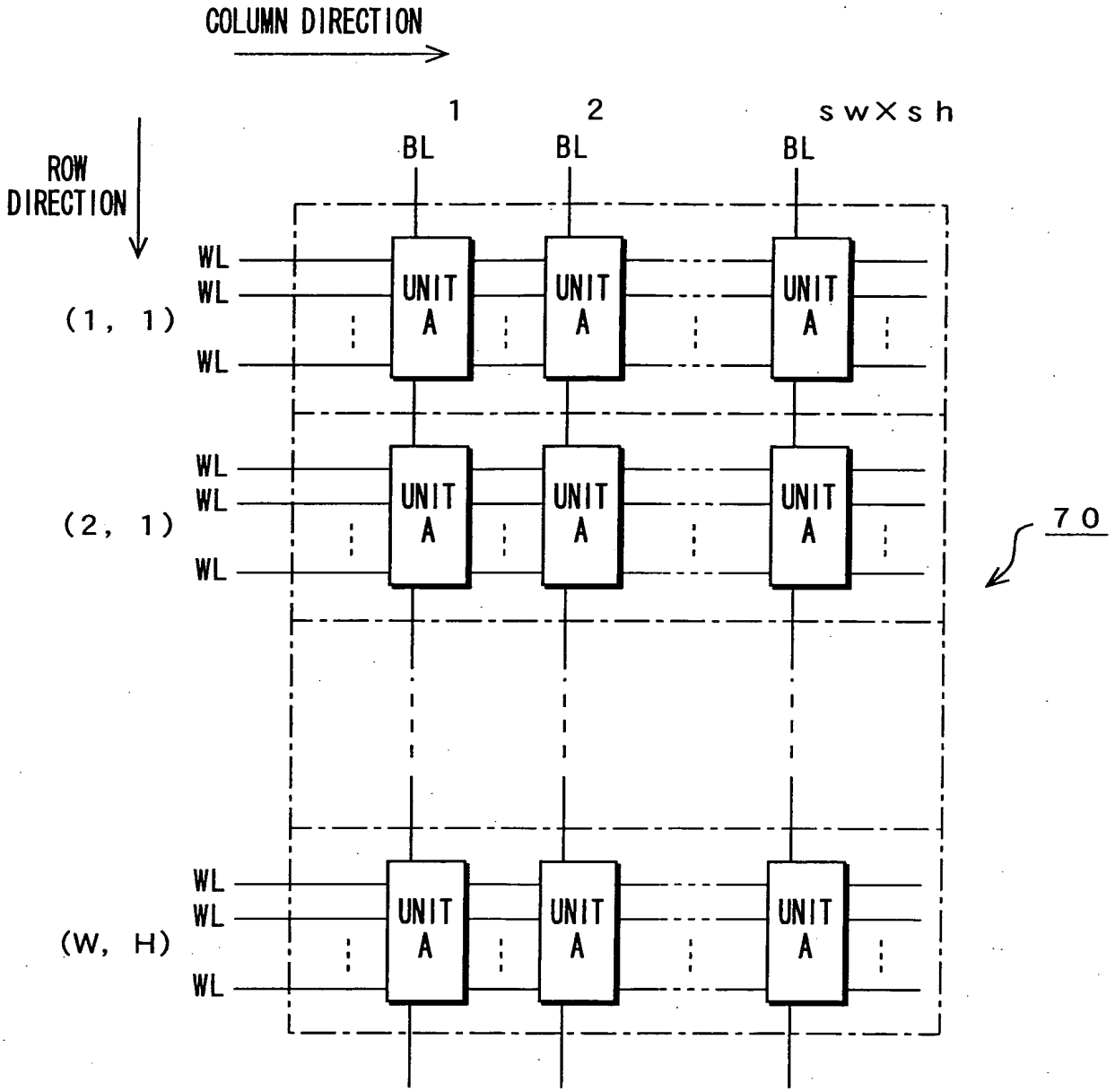

COLUMN DIRECTION
ROW DIRECTION
1
2
sw×sh
BL
BL
BL
WL
WL
WL
(1, 1)
(2, 1)
(W, H)
UNIT A
70

FIG. 22

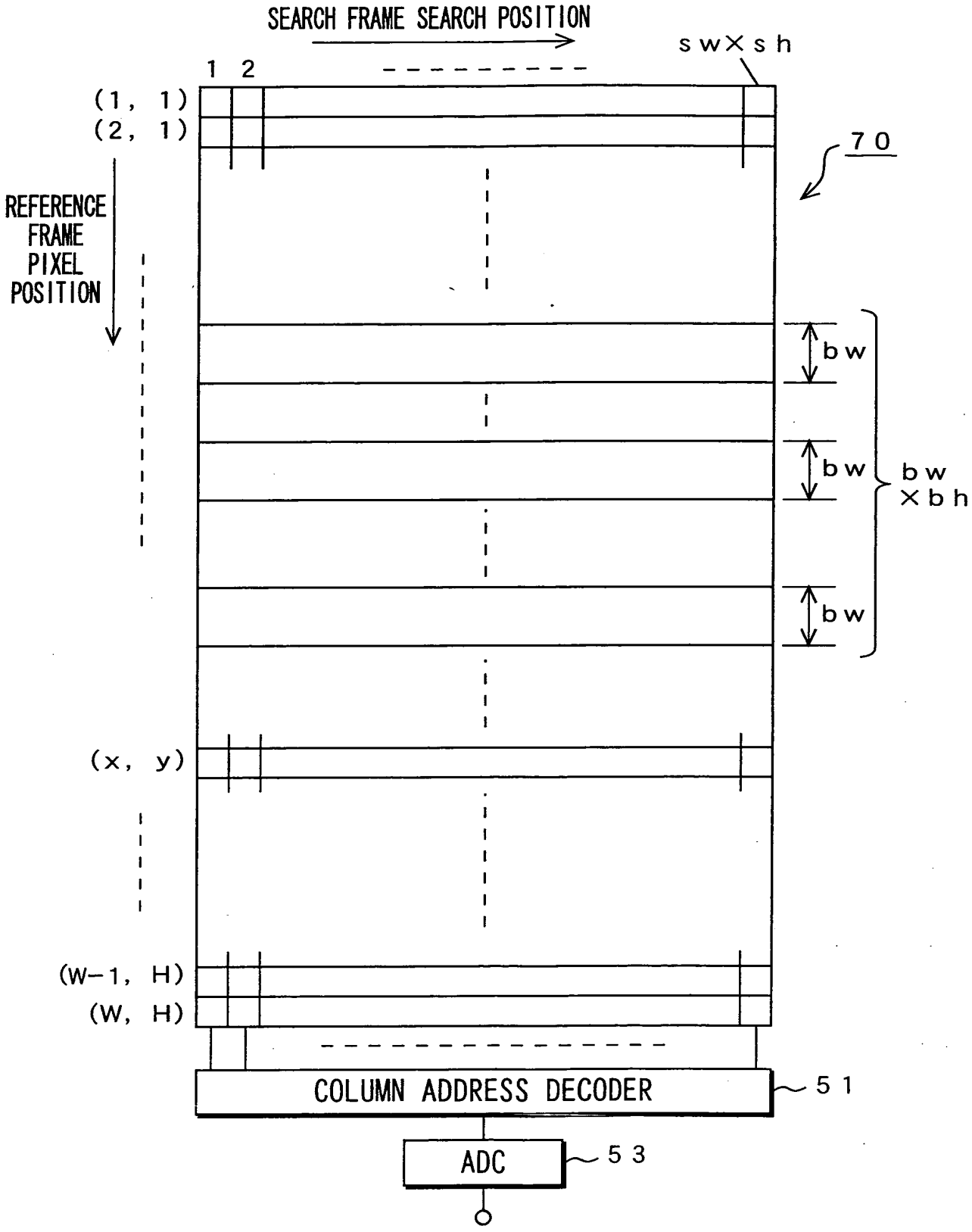

SEARCH FRAME SEARCH POSITION
swxsh
1 2
(1, 1)
(2, 1)
70
REFERENCE FRAME PIXEL POSITION
bw
bw
bw
bw xbh
(x, y)
(W-1, H)
(W, H)
COLUMN ADDRESS DECODER
51
ADC
53
SUM OF ABSOLUTE DIFFERENCE VALUES

FIG. 23

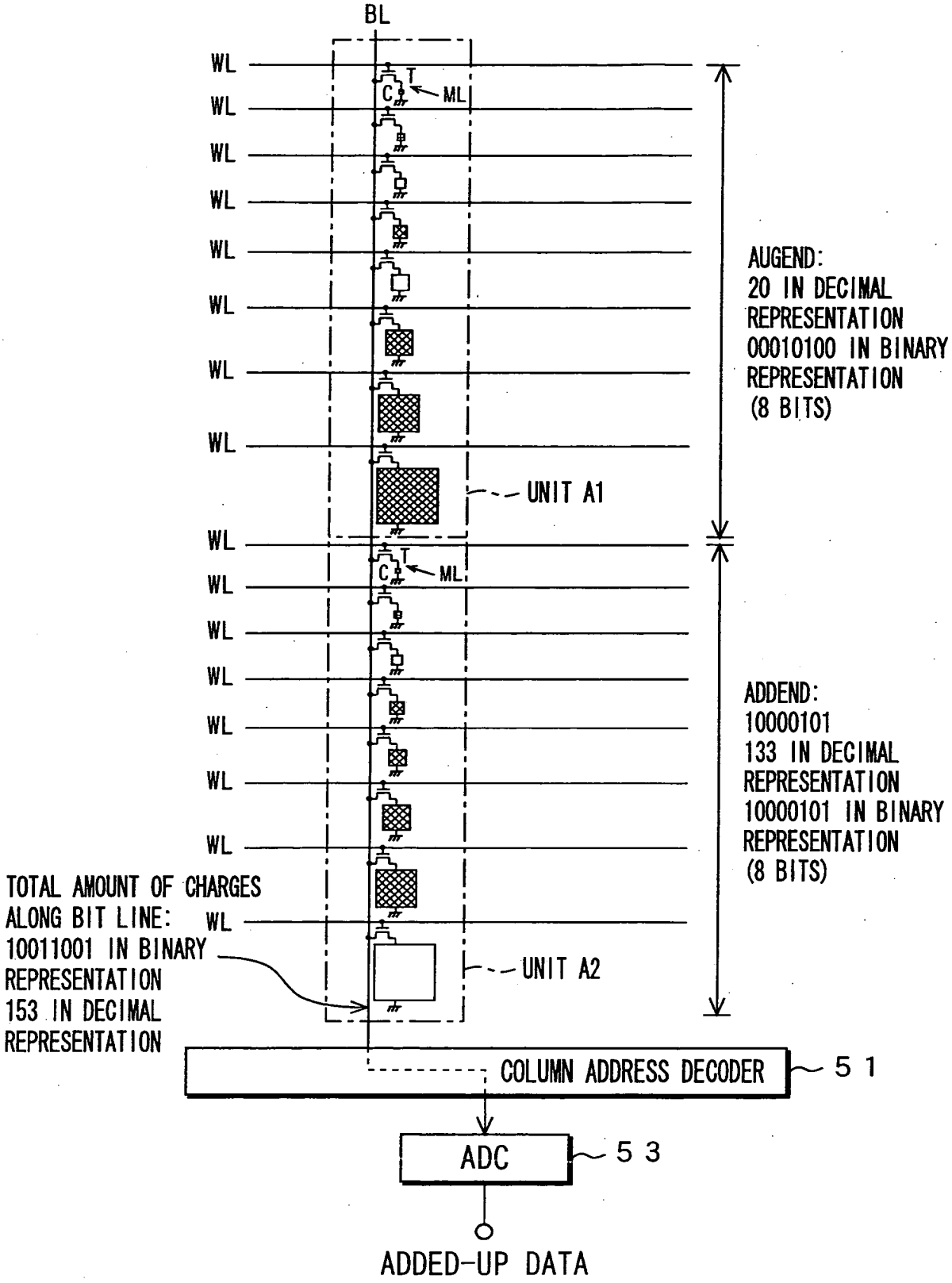

BL
WL
T
C
ML
AUGEND:
20 IN DECIMAL
REPRESENTATION
00010100 IN BINARY
REPRESENTATION
(8 BITS)
UNIT A1
ADDEND:
10000101
133 IN DECIMAL
REPRESENTATION
10000101 IN BINARY
REPRESENTATION
(8 BITS)
TOTAL AMOUNT OF CHARGES
ALONG BIT LINE:
10011001 IN BINARY
REPRESENTATION
153 IN DECIMAL
REPRESENTATION
UNIT A2
COLUMN ADDRESS DECODER
51
ADC
53
ADDED-UP DATA

FIG. 24

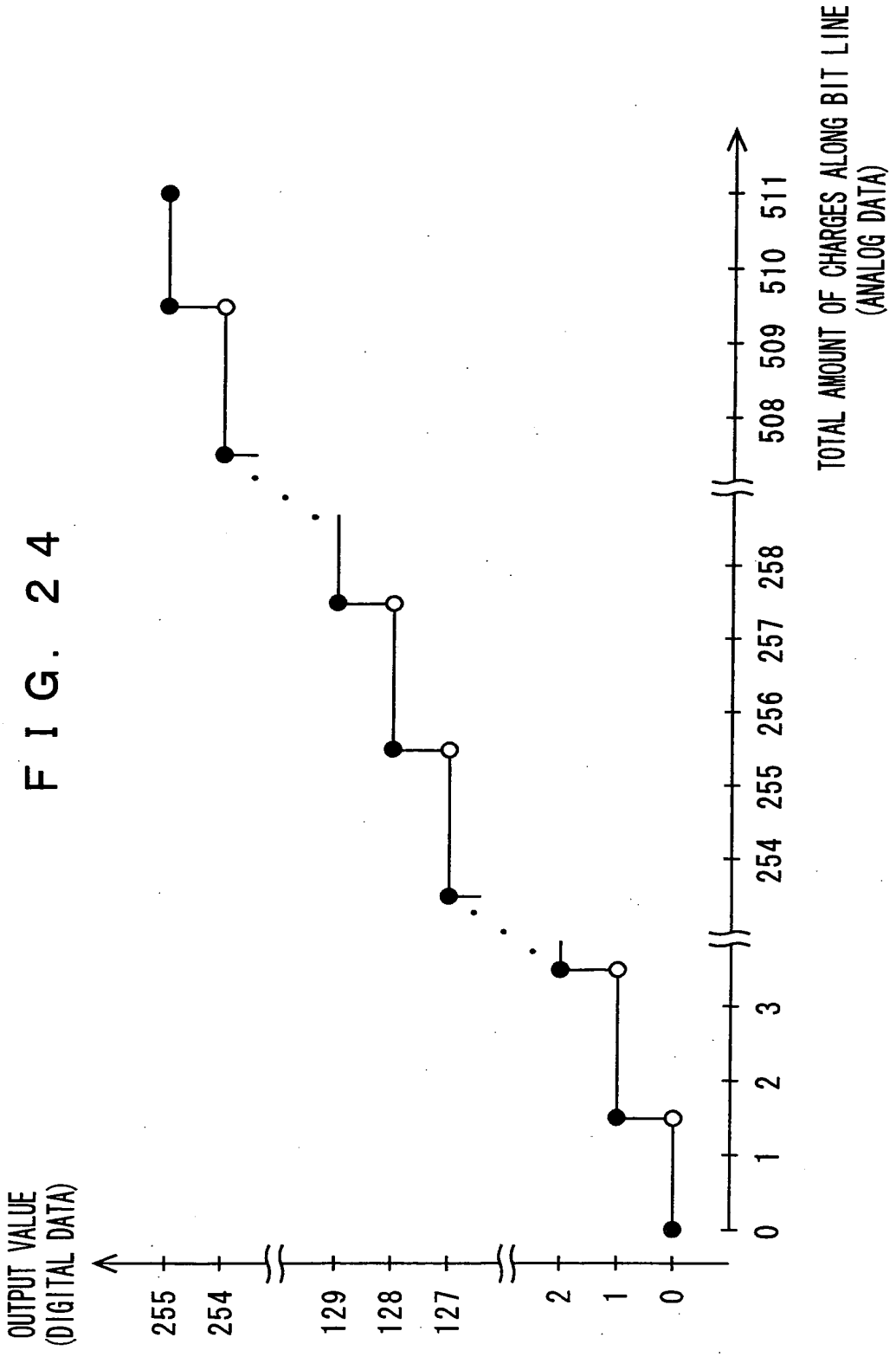
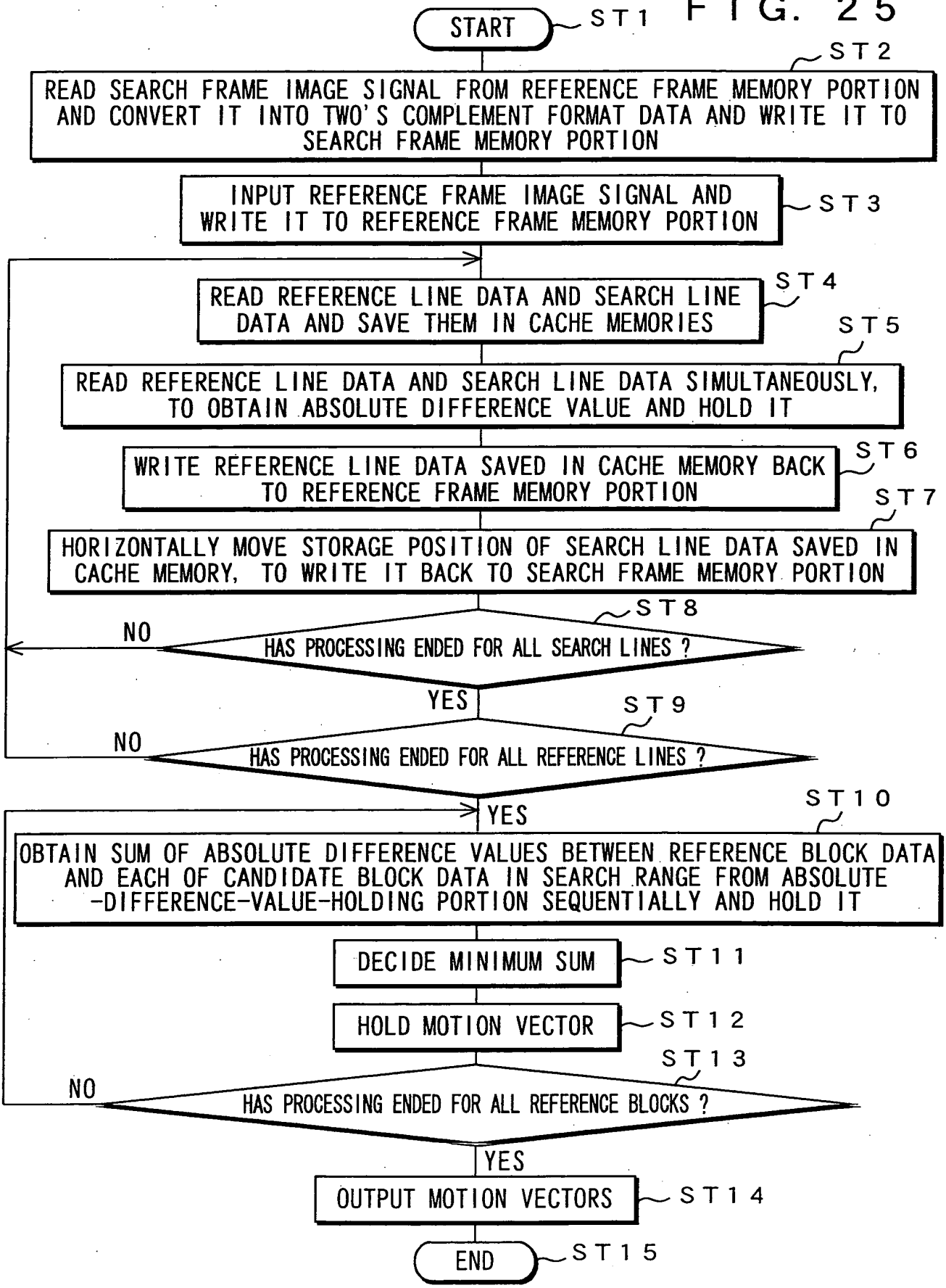

OUTPUT VALUE
(DIGITAL DATA)
255
254
129
128
127
2
1
0
0
1
2
3
254
255
256
257
258
508
509
510
511
TOTAL AMOUNT OF CHARGES ALONG BIT LINE
(ANALOG DATA)

FIG. 25


START
ST1
ST2
READ SEARCH FRAME IMAGE SIGNAL FROM REFERENCE FRAME MEMORY PORTION AND CONVERT IT INTO TWO'S COMPLEMENT FORMAT DATA AND WRITE IT TO SEARCH FRAME MEMORY PORTION
INPUT REFERENCE FRAME IMAGE SIGNAL AND WRITE IT TO REFERENCE FRAME MEMORY PORTION
ST3
READ REFERENCE LINE DATA AND SEARCH LINE DATA AND SAVE THEM IN CACHE MEMORIES
ST4
ST5
READ REFERENCE LINE DATA AND SEARCH LINE DATA SIMULTANEOUSLY, TO OBTAIN ABSOLUTE DIFFERENCE VALUE AND HOLD IT
WRITE REFERENCE LINE DATA SAVED IN CACHE MEMORY BACK TO REFERENCE FRAME MEMORY PORTION
ST6
ST7
HORIZONTALLY MOVE STORAGE POSITION OF SEARCH LINE DATA SAVED IN CACHE MEMORY, TO WRITE IT BACK TO SEARCH FRAME MEMORY PORTION
ST8
NO
HAS PROCESSING ENDED FOR ALL SEARCH LINES ?
YES
ST9
NO
HAS PROCESSING ENDED FOR ALL REFERENCE LINES ?
YES
ST10
OBTAIN SUM OF ABSOLUTE DIFFERENCE VALUES BETWEEN REFERENCE BLOCK DATA AND EACH OF CANDIDATE BLOCK DATA IN SEARCH RANGE FROM ABSOLUTE -DIFFERENCE-VALUE-HOLDING PORTION SEQUENTIALLY AND HOLD IT
DECIDE MINIMUM SUM
ST11
HOLD MOTION VECTOR
ST12
ST13
NO
HAS PROCESSING ENDED FOR ALL REFERENCE BLOCKS ?
YES
OUTPUT MOTION VECTORS
ST14
END
ST15